WHAT IS CLAIMED IS:

1. A bit slice circuit comprising:

a data bus;

a plurality of chips coupled to the data bus, the plurality of chips configured to simultaneously process a slice of data for the data bus, the plurality of chips comprising:

a master chip comprising:

a first time domain circuit operating at a first frequency;

a second time domain circuit operating at a second frequency;

a synchronizing circuit configured to synchronize a signal from the first time domain in the first frequency to the second time domain in the second frequency;

one or more slave chips comprising:

the second time domain circuit operating at the second frequency,

wherein the master chip is configured to send the synchronized signal to one or more slave chips such that the synchronized signal is received in the second time domain circuit for the master chip and the second time domain circuit in one or more slave chips in the same clock cycle.

2. The bit slice circuit of claim 1, wherein the one or more slave chips comprise:

the first time domain circuit operating at a first frequency; and

the synchronizing circuit configured to synchronize a signal from the first time domain in the first frequency to the second time domain in the second frequency, wherein the first time domain circuit and the synchronizing circuit are turned off.

3. The bit slice circuit of claim 1, further comprising a connection wire that routes the synchronized signal from the master chip to the one or more slave chips.

4. The bit slice circuit of claim 3, wherein the plurality of chips comprise a phase circuit that is used to double a width of the synchronized signal before the signal is sent to the one or more slave chips through the connection wire.

5. The bit slice circuit of claim 4, wherein the phase circuit is used to sample a second half of the doubled synchronized signal after the signal is received through the connection wire at the one or more slave chips.

6. The bit slice circuit of claim 1, wherein the synchronized signal received in the second time domain circuit for the master chip is delayed so that the synchronized signal is received in the same clock cycle as the synchronized signal received by the second time domain circuit in the one or more slave chips.

7. The bit slice circuit of claim 1, wherein the master chip and the one or more slave chips comprises an input pin, wherein the input pin is set to a first value for the master chip and a second value for the one or more slave chips.

8. The bit slice circuit of claim 7, wherein the master chip and one or more slave chips include the same circuitry, wherein the input determines if a chip in the plurality of chips is a master chip or a slave chip.

9. The bit slice circuit of claim 1, wherein the master chip and the one or more slave chips comprise a memory, wherein the data bus comprises a first data bus and a second data bus, the data being read in from a first data bus and read out to a second data bus.

10. A bit slice circuit comprising:

a plurality of chips configured to simultaneously process a slice of data for a data bus, the chips including substantially similar circuitry, the plurality of chips comprising:

a first time domain circuit operating at a first frequency;

a second time domain circuit operating at a second frequency;

a synchronization circuit configured to synchronize a signal from the first time domain in the first frequency to the second time domain in the second frequency; and

an input pin configured to be set to a first or second value,

wherein the plurality of chips comprise a master chip with an input pin set to the first value and one or more slave chips with an input pin set to the second value, wherein the master chip is configured to send the synchronized signal to one or more slave chips such that the synchronized signal is received in the second time domain circuit for the master chip and the second time domain circuit in one or more slave chips in the same clock cycle.

11. The bit slice circuit of claim 10, further comprising a connection wire that routes the synchronized signal from the master chip to the one or more slave chips.

12. The bit slice circuit of claim 11, wherein the plurality of chips comprise a phase circuit that is used to double a width of the synchronized signal before the signal is sent to the one or more slave chips through the connection wire.

13. The bit slice circuit of claim 12, wherein the phase circuit is used to sample a second half of the doubled synchronized signal after the signal is received through the connection wire at the one or more slave chips.

14. The bit slice circuit of claim 10, wherein the first time domain circuit comprises a first finite state machine and the second time domain circuit comprises a second finite state machine, the first finite state machine sending the signal that is synchronized for the second finite state machine.

15. The bit slice circuit of claim 10, wherein the input pin determines whether the synchronization signal from the first time domain is received from the master chip if the value is set to the second value or if the synchronization signal is received from the first time domain circuit if the value is set to the first value.

16. The bit slice circuit of claim 10, wherein the master chip and the one or more slave chips comprise a memory, wherein the data bus comprises a first data bus and a second data bus, the data being read in from a first data bus and read out to a second data bus.

17. The bit slice circuit of claim 10, wherein the synchronized signal received in the second time domain circuit for the master chip is delayed so that the synchronized signal is received in the same clock cycle as the synchronized signal received by the second time domain circuit in the one or more slave chips.

18. The bit slice circuit of claim 10, wherein signals from the first time domain and the synchronization circuit of the one or more slave chips are not routed to the second time domain circuit.